What is claimed is:

1. A CMOS image sensor having a plurality of unit cells comprising a photodiode and a plurality of MOS transistors, the plurality of the unit cells being arranged in a matrix array on a semiconductor substrate, wherein

the unit cell comprises a first and a second photodiodes formed on a semiconductor substrate, a first readout transistor connected to the first photodiode and reading out signals thereof, a second readout transistor connected to the second photodiode and reading out signals thereof, a floating diffusion region transmitting the signals and connected to the first and the second readout transistors, a reset transistor connected to the floating region and resetting the potential of the region, an amplifying transistor having a gate connected to the floating diffusion region and amplifying the signals, and a selecting transistor selectively addressing the amplifying transistor,

the unit cell being connected to four address lines, comprising two readout lines of the first and the second readout transistors, a reset line of the reset transistor and a select line of the selecting transistor, all of them extending in the horizontal direction of the matrix arrangement respectively,

the unit cell being connected to a power line connected to the reset transistor and the selecting transistor, and to a signal line connected to the amplifying transistor, both of them extending in the vertical direction of the matrix arrangement

respectively,

the address lines being superimposed in a double-layer every two lines and extended,

the first and the second photodiodes being located apart from each other with the first and the second readout transistors interposed between them,

the floating diffusion region being approximately rectangular, and

the first and the second readout transistors and the reset transistor being connected to respective sides of the floating diffusion region within a semiconductor substrate.

2. The CMOS image sensor as stated in Claim 1, wherein the first and the second readout transistors are connected to sides of the floating diffusion region facing thereto, and the reset transistor is connected to a side interposed by the facing sides.

3. The CMOS image sensor as stated in Claim 1, wherein the first and the second readout transistors are connected to neighboring sides of the floating diffusion region.

4. The CMOS image sensor as stated in Claim 1, wherein the floating diffusion region is constituted to be one of electrodes of the first readout transistor, the second readout transistor and the reset transistor, which is common thereto.

5. The CMOS image sensor as stated in Claim 1, wherein the first and the second readout transistors, the floating diffusion region, the reset transistor, the amplifying transistor and the selecting transistor are located in a region interposed by four gate lines extending respectively in the horizontal direction of the matrix arrangement.

6. The CMOS image sensor as stated in Claim 1, wherein the first and the second photodiodes are located facing to the vertical direction of the matrix arrangement.

7. The CMOS image sensor as stated in Claim 1, wherein the first and the second photodiodes are located facing to the vertical direction of the matrix arrangement and offsetting to each other in the horizontal direction.

8. The CMOS image sensor as stated in Claim 1, wherein the first to the fourth sides of the rectangular floating diffusion region are arranged in approximately 45 degrees to the horizontal direction of the matrix arrangement, the gates of the first and the second readout transistors being arranged to be orthogonal to each other along the neighboring first and second sides, the gate of the reset transistor being arranged facing to the third side, the amplifying transistor being arranged in the direction of the fourth side, and a metal line being pulled out from the floating diffusion region to the gate of the amplifying

transistor.

9. The CMOS image sensor as stated in Claim 1, wherein one of the gate lines of the double layer is the readout line of the first readout transistor and the reset line of the reset transistor.

10. The CMOS image sensor as stated in Claim 1, wherein one of the gate lines of the double layer is the readout line of the first readout transistor and the readout line of the second readout transistor.

11. The CMOS image sensor as stated in Claim 1, wherein the four address lines extending in the horizontal direction of the matrix arrangement are formed by polycrystalline silicon and the two lines extending in the vertical direction are metal.

12. A CMOS image sensor having a plurality of pixel unit cells comprising a photodiode and a plurality of MOS transistors, the pixel unit cells being arranged in a matrix array on a semiconductor substrate, wherein

the unit cell comprises a first and a second photodiodes formed on a semiconductor substrate, a first readout transistor whose source is connected to the first photodiode and reading out signals thereof, a second readout transistor connected to the second photodiode at the source thereof and reading out signals thereof,

a floating diffusion region transmitting the signals and connected to the drains of the first and the second readout transistors, a reset transistor connected to the floating diffusion region at the source thereof and resetting a potential of the region, an amplifying transistor connected to the floating diffusion region at the gate thereof via a metal line and amplifying the signals, and a selecting transistor connected to the source of the amplifying transistor at the drain thereof and addressing selectively the amplifying transistor,

the unit cell being connected to four gate lines, comprising two readout lines of the first and the second readout transistors, a reset line of the reset transistor and a selecting line of the selecting transistor, all of them extending in the horizontal direction of the matrix arrangement respectively,

the unit cell being connected to a power line connected to the drain of the reset transistor and the drain of the selecting transistor, and to a signal line connected to the source of the amplifying transistor, both of them extending in the vertical direction of the matrix arrangement respectively,

the gate lines being superimposed in a double-layer every two lines and extended,

the first and the second photodiodes being arranged apart from each other with interposing the gate lines of the first and the second readout transistors,

the floating diffusion region being approximately rectangular, and

the first and the second readout transistors and the reset transistor being connected to respective sides of the floating diffusion region within a semiconductor substrate.

13. A CMOS image sensor having a plurality of unit cells comprising:

a pair of two photodiodes;

a pair of readout transistors connected to the photodiodes one by one and reading out signals of the photodiodes;

an amplifying transistor amplifying the signals;

a reset transistor resetting the signals; and

a selecting transistor selecting the amplifying transistor,

the plurality of the unit cells being arranged in a matrix array two-dimensionally at a predetermined pitch like approximately a lattice in the vertical direction and the horizontal direction, and respective gates of the pair of the readout transistors, the reset transistor and the selecting transistor being formed by gate lines extending in the horizontal direction of the matrix arrangement, wherein

the gate lines form a double-layered line layer in which at least two lines thereof are superimposed together in the layer direction,

the two photodiodes of the unit cell being located apart from each other in the vertical direction of the matrix arrangement, the pair of the readout transistors sharing a floating diffusion

region to become a drain and being located between the two photodiodes,

the floating diffusion region being formed in an approximately rectangular shape, and

the reset transistor being provided directly adjacent to the floating diffusion region.

14. The CMOS image sensor as stated in Claim 13, wherein the gates of the pair of the readout transistors are located to be orthogonal to each other along neighboring sides of the rectangular floating diffusion region, the pair of the photodiodes being located horizontally in the direction of approximately 45 degrees to the gates of the readout transistors, the gate of the amplifying transistor being located in the direction of one of the remaining sides of the floating diffusion region that are not covered by the gates of the reset transistor, and a line being pulled out from the floating diffusion region to the gate of the amplifying transistor.

15. A CMOS image sensor having a plurality of unit cells comprising:

a pair of two photodiodes;

a pair of readout transistors connected to the photodiodes one by one and reading out signals of the photodiodes;

an amplifying transistor amplifying the signals;

a reset transistor resetting the signals; and

a selecting transistor selecting the amplifying transistor,

the plurality of the unit cells being arranged in a matrix array two-dimensionally like approximately a lattice at a predetermined pitch in the vertical direction and the horizontal direction, wherein

the two photodiodes of the unit cell are located apart from each other in the vertical direction of the matrix arrangement, the pair of the readout transistors sharing a floating diffusion region to become a drain and being positioned between the pair of the photodiodes, and the gates of the pair of the readout transistor being located to correspond to respective photodiodes,

the floating diffusion region being formed in an approximately rectangular shape,

the reset transistor being located directly adjacent to the floating diffusion region,

readout lines constituting respective gates of the readout transistors corresponding to respective photodiodes being positioned in parallel together to interpose the floating diffusion region from the both sides of the vertical direction, and

the amplifying transistor, the reset transistor, and the selecting transistor being all formed in a region interposed by the readout lines of the pair of the readout transistors.

16. The CMOS image sensor as stated in Claim 15, wherein

respective gates of the readout transistors corresponding to the photodiodes of the unit cells are located to be orthogonal to each other along neighboring sides of the approximately rectangular floating diffusion region, and the reset transistor is provided adjacent to the floating diffusion region.

17. The CMOS image sensor as stated in Claim 15, wherein the centers of the pair of the two photodiodes adjacent to the matrix in the vertical direction are horizontally offset to each other.